Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		(operating adj1 mode$1) and ((address adj1 size) and (operand adj1 size))	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:09
		(operating adj1 mode) near4 indicators	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:09
L1	278	(712/229).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/05/16 13:58
L2	205	(712/43).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/05/16 13:58
L3	2	(address$3 near4 siz$3) near4 (enabl$3 near4 pag$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/16 13:59
L4	2	(address$3 near4 siz$3) with (enabl$3 near4 pag$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/16 13:59
L5	15	(address$3 near4 siz$3) same (enabl$3 near4 pag$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/16 14:00
L6	40	(address$3 near4 siz$3) same (enabl$3 with pag$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/16 14:01
L7	4	(address$3 adj1 siz$3) same (enabl$3 with pag$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/16 14:02
L8	35	(address$3 adj1 siz$3) same (enabl$3 same pag$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/05/16 14:02
S1	357	mode adj1 indicators	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:07

S2	63	(operating adj1 mode) and (mode adj1 indicators)	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:08
S3	63	(operating adj1 mode) and (mode adj1 indicators)	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:08
S4	26	processor and (operating adj1 mode) and (mode adj1 indicators)	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:08
S5	8	(operating adj1 mode) near4 (mode adj1 indicators)	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:08
S6	231	(operat$4 adj1 mod$2) near4 (mod$2 adj1 bit$1)	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:09
S7	113	(operating adj1 mode) and (("16" adj1 bits) near4 ("32" adj1 bits))	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:09
S8	81	(operating adj1 mode$1) and (mode adj1 indicators)	US-PGPUB; USPAT; JPO; DERWENT	OR	OFF	2004/05/26 15:09
S9	42	processor and (operating adj1 mode$1) and (mode adj1 indicators)	US-PGPUB; USPAT; JPO; DERWENT	OR`	OFF	2004/05/26 15:09
S10	3	(segment adj1 selector$1) near4 (entries)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:13
S11	0	(adjacent adj1 memory adj1 locations) near4 (64?bit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:16
S12	0	(adjacent adj1 memory) near4 (64?bit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:15
S13	0	(adjacent adj1 memory) near4 ("64" adj1 bit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:16

S14	35	(memory adj1 locations) near4 ("64" adj1 bit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:15
S15	335	adjacent adj1 memory adj1 locations	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:16
S16	0	(adjacent adj1 memory adj1 locations) near4 (large adj1 data)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:31
S17	73	(adjacent adj1 memory adj1 locations) near4 (data)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:18
S18	27	(floating adj1 point) near4 (memory adj1 locations)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:19
S19	0	(memory adj1 locations) near4 (large adj1 data)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:32
S20	7	(memory adj1 locations) with (large adj1 data)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:36
S21	26	(memory adj1 locations) same (large adj1 data)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:47
S22	120	(double adj1 word) near4 storage	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:52
S23	11	(double adj1 word) near4 storage near4 locations	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 15:52
S24	827	instruction adj1 translat$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 16:02
S25	4	software near4 instruction adj1 translat$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 16:02

S26	0	software adj1 instruction adj1 translat$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 16:02
S27	13	software near4 (instruction adj1 translat$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/05/26 16:02
S28	242	(712/229).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/06/28 07:59
S29	190	(712/43).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/06/28 07:59
S30	3289	pag$3 near4 segment$4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/06/28 08:00
S31	273	paging near4 segmentation	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/06/28 08:00
S32	0	(paging adj2 addresses) near4 (segmentation adj1 memory)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/06/28 08:01
S33	9	paging near4 (segmentation adj1 memory)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/06/28 08:21
S34	232	paging near2 segmentation	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/06/28 08:22
S35	267	(712/229).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/12/09 13:51
S36	198	(712/43).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2004/12/09 13:51

| S37 | 272 | (712/229).CCLS. | US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB | OR | OFF | 2005/04/04 07:37 |
| S38 | 203 | (712/43).CCLS. | US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB | OR | OFF | 2005/04/04 07:37 |

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Home Networking with IEEE 802.15. 4: A Developing Standard for Low-Rate Wireless Personal Area ...
B Heile, A Technologies, V Bahl, P Semiconductors - Cited by 29 - Web Search
... quality **indication**, and channel switching, which **enable** channel assess ... or multihop
applications with more **address** overhead, may require larger packet **sizes**. ...
IEEE Communications Magazine, 2002 - ieeexplore.ieee.org - geocities.com - coe.uncc.edu - cs.ucla.edu - all 8 versions »

Use of superpages and subblocking in the **address** translation hierarchy
M Talluri, MD Hill - View as HTML - Cited by 14 - Web Search
... This is analogous to an increase in disk **paging** if the working set is larger ... Third,
larger virtual and physical **address sizes**, eg, 64-**bit** virtual addresses ...
Computer Sciences Technical Report - 206.231.101.22 - solarisinternals.com - cs.wisc.edu - portal.acm.org - all 8 versions »

On Demand **Paging** Using Bluetooth Radios on 802.11 Based Networks
Y Agarwal, RK Gupta, T Report - View as HTML - Cited by 2 - Web Search
... **address** associated with the destination IP **address** and sends ... downloaded and uploaded
a few files of varying **sizes**. ... This would **enable** the clients to be able to ...
Center for Embedded Computer Systems, UC Irvine, UC San ..., 2003 - mesl.ucsd.edu - cecs.uci.edu - ics.uci.edu - ics.uci.edu

[PS] Flexible Physical Memory Management
D McNamee, G Exam - View as HTML - Web Search
... Matching page **sizes** to client ... object corresponding to the client's virtual **address**
and requests ... replacement algorithm), or with normal locality (to **enable** LRU ...
cs.washington.edu

[PS] Evaluation of architectural support for global **address**-based communication in large-scale parallel ...
A Krishnamurthy, KE Schauser, CJ Scheiman, RY Wang ... - View as HTML - Cited by 22 - Web Search
... and (3) a re- sponse or completion **indication** is delivered ... I/O bus supports only
28-**bit** addresses, only a ... the remote node has extended its **address** space beyond ...
Computer Architecture News, 1996 - http.cs.berkeley.edu - arch.cs.ucdavis.edu - lambda.cs.yale.edu - cs.ucsb.edu - all 14 versions »

Bluetooth: Vision, Goals, and Architecture
I Vision - View as HTML - Web Search
... in Section I, the SIG wants to **enable** the following ... and encryption proce- dures Entity
Size Bluetooth **address** 48 bits ... three entities and their **sizes** as used in ...
metc.pku.edu.cn - cnscenter.future.co.kr - cise.ufl.edu - grc.upv.es - all 19 versions »

[PS] Further Pipelining and Multithreading to Improve RISC Processor Speed. A Proposed Architecture and ...
B Goossens, DT Vu - View as HTML - Web Search
... or a write **enable** (store instruction) or a data cache ... the instruction and data internal
caches **sizes**, given in ... at least 48 bits target absolute **address** may be ...
PaCT, 1995 - gala.univ-perp.fr - portal.acm.org

Improving the performance of SML garbage collection using application-specific virtual memory ...
E Cooper, S Nettles, I Subramanian - Cited by 12 - Web Search
... We changed the strategy for determining the **sizes** of the ... map the object into the
client's **address** space. ... request from the kernel as an **indication** that memory ...
LISP and Functional Programming, 1992 - portal.acm.org - portal.acm.org - csa.com

Remembrance of Things Past: Locality and Memory in BDDs
S Manne, D Grunwald, F Somenzi - Cited by 8 - Web Search
... In Section 4 we **address** the question of whether the DFS ... To **enable** reasonable comparisons
to the results in 10 , the experimental setup ... for a variety of **sizes**. ...
DAC, 1997 - portal.acm.org - acm.org - sigda.org - ieeexplore.ieee.org - all 7 versions »

Evaluation of Architectural Support for Global **Address**-Based Communication in Large-Scale Parallel ...
RY Wang, DE Culler, K Yelick - Web Search
... and (3) a re- sponse or completion **indication** is delivered ... I/O bus supports only
28-**bit** addresses, only a ... the remote node has extended its **address** space beyond ...
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Bluetrees-Scatternet Formation to **Enable** Bluetooth-Based Ad Hoc Networks
GV Zaruba, S Basagni, I Chlamtac - <u>View as HTML</u> - <u>Cited by 103</u> - <u>Web Search</u>
Bluetrees—Scatternet Formation to **Enable** Bluetooth-Based Ad ... and identities (ie, the
Bluetooth **address**) of each ... be read for different network **sizes** with nodal ...
Proc. IEEE ICC, 2001 - tik.ee.ethz.ch - <u>csie.ncnu.edu.tw</u> - <u>ieeexplore.ieee.org</u>

Sharing and protection in a single-**address**-space operating system
JS Chase, HM Levy, MJ Feeley, ED Lazowska - <u>Cited by 164</u> - <u>Web Search</u>
... any case, it is clear that **address sizes** have leaped ... Sharing and Protection in a
Single **Address** Space ... operating systems, and language technology **enable** us to ...
ACM Transactions on Computer Systems, 1994 - portal.acm.org - <u>cs.nyu.edu</u> - <u>paul.rutgers.edu</u> - <u>www-csl.cs.colorado.edu</u> - <u>all 10 versions »</u>

User-level management of kernel memory
A Haeberlen, K Elphinstone - <u>Cited by 3</u> - <u>Web Search</u>
... Linux server have atypical resident set **sizes** because they ... in our experiment) mapped
to their **address** spaces ... Kpagers should also **enable paging** of kernel data to ...
Proc. of the 8th Asia-Pacific Computer Systems Architecture ... - springerlink.com - <u>kevine.web.cse.unsw.edu.au</u> - <u>l4ka.org</u> - <u>i30www.ira.uka.de</u> - <u>all 11 versions »</u>

ATUM: A New Technique for Capturing **Address** Traces Using Microcode
A Agarwal, RL Sites, M Horowitz - <u>Cited by 132</u> - <u>Web Search</u>
... Sample **sizes** of a million references are feasible, and ... locations were modified to
record the **address** trace ... We wrote a Pascal program to **enable** tracing, wait for ...
ISCA, 1986 - portal.acm.org - <u>portal.acm.org</u>

[PS] A High Resolution MMU for the Realization of Huge Fine-Grained **Address** Spaces and User Level Mapping
J Liedtke, GMDTR No - <u>View as HTML</u> - <u>Cited by 5</u> - <u>Web Search</u>
... several **sizes** (in the extreme case all **sizes**) would have ... level and/or returned as
a real **address**. ... As shown in [3], 8-associative guarded page tables **enable** an ...
German National Research Center for Computer Science ..., 1994 - tu-chemnitz.de

A Flexible External **Paging** Interface
YA Khalidi, MN Nelson - <u>View as HTML</u> - <u>Cited by 12</u> - <u>Web Search</u>
... the bind call (and the corresponding **address** space map ... To **enable** caching of file
attributes and read/write ... serviced by the CFS, and all **paging** operations go to ...
USENIX Microkernels and Other Kernel Architectures Symposium, 1993 - research.sun.com - <u>sunlabs.com</u> - <u>cs.fau.de</u> - <u>informatik.uni-erlangen.de</u> - <u>all 11 versions »</u>

Use of superpages and subblocking in the **address** translation hierarchy
M Talluri, MD Hill - <u>View as HTML</u> - <u>Cited by 14</u> - <u>Web Search</u>
... One way to increase the **address** space mapped by a ... in Alpha, virtual and physical
mem- ory **sizes** have increased ... Extra **paging** in small-memory ma- chines from use ...
Computer Sciences Technical Report - 206.231.101.22 - <u>solarisinternals.com</u> - <u>cs.wisc.edu</u> - <u>portal.acm.org</u> - <u>all 8 versions »</u>

[PS] Porting NetBSD to the AMD x86-64: a case study in OS portability
F van der Linden - <u>View as HTML</u> - <u>Cited by 1</u> - <u>Web Search</u>
... Assumptions made about type **sizes** on 32-bit plat- forms were a large problem when
64-bit platforms came ... 1. **Enable** Physical **Address** Extensions ... 4. **Enable paging** ...
Proceedings of the BSDCon 2002 Conference - usenix.org - <u>usenix.org</u> - <u>portal.acm.org</u>

[PS] A Concurrent Programming Environment for the i486
AA Froehlich, H Savietto, L Piccoli, RB Avila - View as HTML - Cited by 2 - Web Search
... In this mode, memory segments have variable **sizes** in bytes ... Actually, only two flat
(entire **address** space) i486 ... to each logical segment that **enable** or disable ...
inf.ufsc.br - inf.ufrgs.br - gppd.inf.ufrgs.br - lisha.ufsc.br

Understanding Solaris Filesystems and **Paging**
JL Bertoni - View as HTML - Cited by 6 - Web Search
... to disk with an indirect block **address** in place ... It is controlled by an **enable** switch,
freebehind , that ... cannot be changed, its input-output **sizes** will inuence ...
Technical Report TR-98-55, Sun Microsystems, 1998 - sunlabs.com - research.sun.com - sunlabs.com - research.sun.com - all 5
versions »

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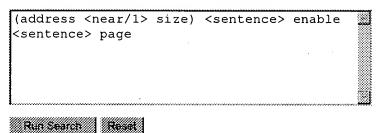
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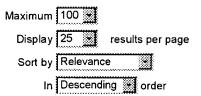   ☑ IEE Conference Proceedings
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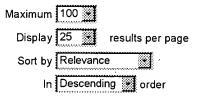**» Select date range**

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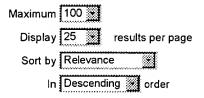

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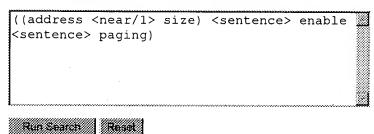
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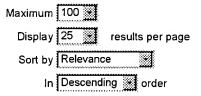
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